

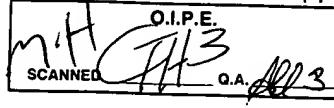
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J1036 U.S. PTO
09/883210
06/19/01

	Subclass	ISSUE CLASSIFICATION
	Class	

PATENT NUMBER

U.S. UTILITY Patent Application

	O.I.P.E.	PATENT DATE
	Q.A. 12/3	

APPLICATION NO. 09/883210	CONT/PRIOR F	CLASS 257	SUBCLASS 750	ART UNIT 281	EXAMINER Nguyen
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APPLICANTS
Hiroyuki Nitta
Yoshiaki Fukuzumi
Yusuke KohyamaTITLE
Semiconductor device having a wiring layer of damascene structure
and method for manufacturing the samePTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)			
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)		
INTERNATIONAL CLASSIFICATION					
<input type="checkbox"/> Continued on Issue Slip Inside File Jacket					

TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	(Assistant Examiner) _____ (Date) _____			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____				ISSUE FEE	
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